PanSTARRS Detector Controller Electronics Development Plan

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1. Revision Log

Rev 0.	First draft	PMO
Rev 0.1	Added JTAG programmer, CPU COTS board Development System section , laminar flow hood in Lab section.	PMO
Rev 0.2	Added Purchase and Tracking section, mod physical requirements	PMO
Rev 0.3	Added PreCODR graphics	PMO

2.Abstract

This is a working document intended to provide an overview of the development plan for the PanSTARRS detector electronics system. For the immediate future, detailed information will be included in this plan that will be broken out into other documents at a later date. Estimates for project phases, labor, organizational resources, component costs and schedule milestones are given.

3. Introduction

The combined demands of the high pixel count and desired small form factor of the PanSTARRS detector controller system makes existing CCD/array controller designs inappropriate. Although the IfA has a proven track record producing facility class electronics instrumentation, it is prudent to write a written plan for both the development and production plan phases for the PanSTARRS project

4. Overall Plan and Phases

The four major project phases of Development, Production, Integration and Deployment can be further broken down into these sub-areas:

The end goal of the Development phase is to design and produce a detector controller capable of running a 1 x 4 assembly of OTA's in a form factor suitable for testing in a laboratory and on a telescope.

- Development Phase
  - Requirements derivation
  - Conceptual design
  - Infrastructure setup
  - Development Plan
  - Development system work
    - Specify and Assemble

        - Metrics testing
        - Hardware and software development
    - Custom components
        - Design
        - Fabricate
        - Test and integrate
    - Testing
        - Centroid OTA clocking benchtest
        - ADC analog testing
        - DAC testing
    - System integration
        - Interface identification
        - Technical interchange meetings
        - Interface control documents
    - Project requirements
        - Milestone identification
        - Scheduling
        - Cost estimates and tracking
        - Infrastructure and resource management
    - Technical oversight
        - Review and approval

The goal of the Production phase is to fabricate electronics for four fully functional gigapixel OTA cameras. Production schedule will allow the systems to be produced in a serial fashion.

- Production Phase
    - Requirements review
    - Plan proposal
        - Cost engineering
        - Resource estimate
        - Infrastructure tradeoffs
    - Review and Approve
    - Redesign
        - Engineering changes
        - System requirements incorporation
        - Vendor upgrades
    - Fabrication plan
        - Contract manufacturing study
        - Subassembly test plan
        - Infrastructure identification
        - Budget
    - Fabrication and Test
        - Contracted test fixtures and software design
        -
    - System Integration

5. Requirements Derivation

Electrical requirements will be derived from a combination of science requirements analysis and technical interchange meetings. Lower level functional and performance requirements can be derived after a conceptual design is finalized.

5.1. Modes of Operation

The OTA will be operated in a sequence of different modes of clocking and readout to accomplish the overall goal of a corrected science image. The OTA design incorporates specific circuitry that will need to be serviced by the controller electronics to accomplish these modes.

Mode Name	**Description**	**OTA operation**	**Controller Function Required**
Idle	No integration, no guide	Resets?	Reset OTAs?
Shutter Control Mode	No integration, no guide		
Guide Star Acquisition mode	~1 sec Integration ~0.5 sec Readout for ~ 5 guide objects in 5 cells per OTA	Integrate Address cells Clock out	Reset, Integrate timing, Readout, Transport data to Host computer, Host computer determines centroids and corresponding clocking patterns for image correction.
Combined Guide and Integration Mode	Fast clocking and readout of Guide cells	Integrate Address cells Clock out	
Low Noise Readout Mode	(Closed shutter) readout of science image	Integrate Address cells Clock out	

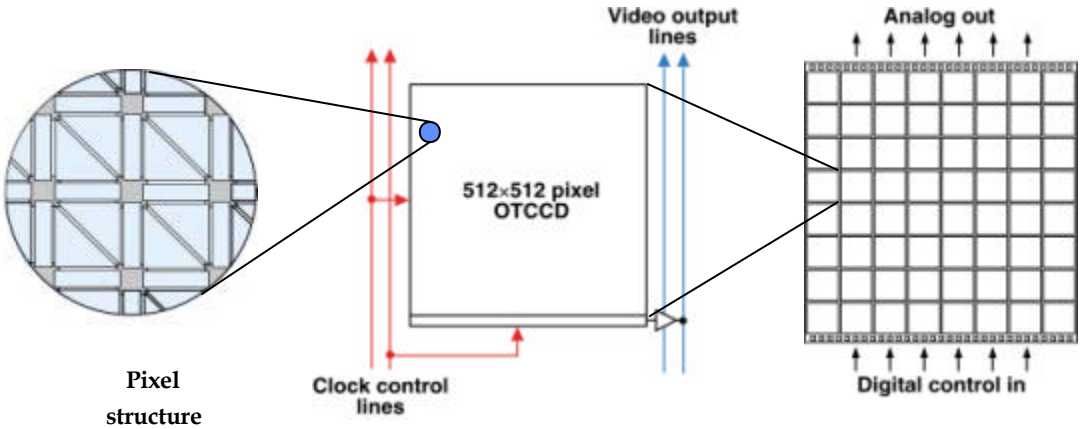
The typical sequenced readout of an OTA would be

Sequenced readout :

- Open Shutter (trigger or delay?)
- Acquire
  - ~1 sec integration, readout ~0.5sec
  - Host determines ~5 guide objects in 5 cells per OTA
- Guide + Integration
  - ~5 guide cell subarray readout at 10-30Hz (<100Hz)
  - host centroids and determines guide subarray position
  - Host also computes OT parallel shift patterns for remaining cell
    - Expected Itimes Nominal 10s of seconds
      - Max ~1000sec
      - Min ~shutter speed/setup
- Apply OT parallel shift clocks (~10usec each)
- Delay ~50msec
- Close shutter and Readout ~2sec

5.2. Basic OTA functionality

The overall structure of the OTA is shown in the next diagram. See appendix A. for detailed specifications for the OTA.



The inputs and outputs of the OTA can be logically broken up into the following areas. *OUTPUTS

Function	*Name*	*Count*	*Voltage*	*Speed*	*Switched?*	*Current*
Clocking	Serial	8	0 to +6-7V	~100nsec	fast	small
Clocking	Parallel	5	0 to +10V	~300nsec?	fast	large
Clocking	scupper	1	O to +2V	DC	bias	~15uA
Clocking	substrate	2	0V	DC	bias	
Bias	Extra bias 1	2	-30V to -40V		Medium?	~uA
Bias	Channel Stop	2	0V	DC	bias	
Bias	Extra bias 2	3	-30 to +15V	DC	bias	~uA
TOTAL		78				

5.3. Electronics Hardware Performance Requirements

The following table summarizes the performance requirements for different parts of the system.

Driver>	Camera Control	Image Frame readout	Guide rate	Guide Box size	Image size	Full well	Read Noise	Power Dissipation
Affected Area		2 to 10sec 2sec goal	10-30Hz 100Hz goal	32 x32 pixels	1Gpixel 2Gbytes	100K e	4e- @ 1MHz 2e- @ 100kHz	Max? Active cooling required
Synchronized OTA clocking	50nsec <30 sec goal							
Centroid and clock modify latencv	2msec <2msec goal		2msec <2msec goal					
Clock time resolution	50nsec <30nsec goal							
ADC resolution						>14 bits 16 bits goal	>14 bits 16 bits goal	
Signal Chain and ADC speed		1usec/ conversion <1 usec goal		9.77usec				
System Noise	Crosstalk <1LSB						1LSB < 1 e	
Image Memory					2Gbytes			
Data buffer					4Gbytes 8Gbytes goal			
Internal data transport		~214Mbps min 8Gbps						
External Data Transport		8Gbps						

5.3.1. Full Camera operation

- Synchronized clocking to <30nsec.
- Heat dissipation from controller system should not impact seeing.

- System will need active cooling.
- System goal of < 400Watts (On Telescope, per Gigapixel Camera).
- Noise floor 1 LSB, less than 1e-.
- OTA crosstalk must be less than noise floor
- Data export = ?

5.3.2. OTA Input and Control

- Sequenced readout
- guide rates 10-30Hz
- Nominal guide patch ? X ?
    - @ 0.3 arcsec/pixel 10 arcsec patch = ~32 X 32 pixels, 10msec/1024 pixels = 9.77 usec/pixel max speed clock+signal condition+ADC+buffer
- Centroid and shift calculation time + Change clock patterns, latency goal = 2msec goal
- Clocking pattern time resolution ~10nsec

5.3.3. OTA Output

- 100K e- well and expected 4e- noise at 1 MHz
- 2e- noise goal at 100 kHz (guiding)
- ADC bit resolution – approx two bits on the noise
    - 100k / 4 = 25K X 2 = 50K resolution wanted
        - 16 bits = 64K
        - 14 bits = 16K
        - Want > 14bits
- Image memory
    - OTA 4096 x 4096 pixels = 16M pixels = 32MBytes (16 bit resolution)
    - 8 x 8 focal plane = 1Gpixel = 2Gbytes (16bit)
- Data buffering and storage
    - Unless data transport is real time, minimum storage is 2Gbytes, 4Gbytes double buffered.
- Memory access speed minimum ~8 to 16Gbits/sec (1 to 2 Gbytes/sec).
- Full 1Gpixel focal plane readout in ~2sec = ~8Gbits/sec
- Signal processing chain
    - 1Gpixel / 64 OTA = 16Mpixels / OTA
    - 16Mpixels / 8 outputs = 2Mpixels /output
    - 2 sec / 2Mpixels = 954nsec/pixel
    - ADC speed
    - ADC plus settle time ~1usec per output
    - 1Mhz ADC borderline too slow (unless CDS built-in)
- Controller data transport
    - Maximum speed matches Full 1Gpixel focal plane readout in ~2sec = ~8Gbits/sec
    - Minimum speed equal to shortest expected science integration ~10s = 214 Mbits/sec
- Internal (controller) data path >= 8Gbits/sec
- Path to Host(s) >= 8Gbits/sec

5.3.4. Internal Data Throughput Requirements

Stage	*Array/ADC Readout*	*CompactPCI Bus*	*COTS CPU*	*1G ethernet*	*Pixel Processor*	*Data Storage*
Requirement	Min 64MBps Goal 128MBps	Min 64MBps Goal ≥128MBps	Min ≥ 128MBps	Min 64MBps Goal ≥128MBps	Min ≥ 128MBps	Min 64MBps
Capability	Max 260MBps (5MSps/ADC x 24)	132MBps theoretical (32 bit) 265MBps (64 bit) *noise & ground isolation	Processor/ memory access (read + write)	125MBps theoretical	Processor/ memory access (read + write)	Burst ~60MBps Only ~20MBps sustained
Notes	33.55 Mpixel/sec (~2sec)		Test to confirm	Use dual 1Ge?	133/400/533Mhz FSB	Duty cycle?

5.4. Physical Requirements

5.4.1. Telescope Mounted Subassembly:

The overall envelope limits for the electronics system is defined by the entire focal plane size and the telescope design. The baseline design goal is to be able to scale multiple copies of the controller and still fit roughly in the shadow of the telescope primary mirror support and focal plane. These overall dimensions are: H x W x D.

Present placeholder values: each set of focal plane electronics to be mounted in 19 inch rackmount chassis. Each rack must hold 8 IOTA's each. Per telescope, quantity 2, 4U Elma Type 11C CPCI chassis. (1U = 1.65 inches) 6.6"H x 16.8"W x 12"D.
Per Telescope Dimensions:13.2"H x 16.8"W x 12"D.
Per Telescope Weight: estimated 40lbs.
Cooled Air Supply and warm air removal: Design is TBD, need to estimate CFM ratings for example forced air cooling system.

5.4.2. Power Supply Subassembly

Each Telescope will need an array electronics power supply for the noise sensitive telescope mounted electronics.

Present placeholder: Agilent 66000 system power supply full populated with modules.
Per Telescope Dimensions: 178mmH x 426mmW x 678mm, (7"H x 16.75"W x 26.7"D).
Per Telescope Weight: estimated 80lbs.

Acceptable cable length to Telescope mounted Subassembly = 15 ft.

5.4.3. Pixelserver Subsystem

Standard 19 inch racks will house the ~16 1U computers (per telescope = 64 total), plus rack space for 1Gethernet switches and temperature controllers (and UPS??).

5.5. Environmental Requirements

TBD

5.6. Power Dissipation and Supply Requirements

The goal here is to keep the power dissipation of the system low enough to not adversely impact the seeing environment. Early estimates indicate that some form of active cooling will be necessary to remove the heat generated by the electronics. Previous designs delivered by the IfA to Mauna Kea observatories have used a ~1KW cooling budget (per cooled enclosure) based on a glycol flow rate from standard chillers. Actual spec: FILL IN.

The estimated system total for 1 and all 4 systems is: TBD.
And will require UPS and non UPS facility power of: TBD Note Webpage requirement of 1000W is inadequate. Rough estimate ~4KW.

5.7. Software Requirements

CPU Board

I. System Requirements

A. High Level

1. The CPU Board set up DMA transfers of data from the FPGA Board to the CPU Board main memory.
2. The CPU Board will send the data in main memory over a high speed link to the PixelServer system.
3. The CPU Board will calculate the centroid of our reference object and produce correction patterns which it will send to the FPGA Board.
    a. These correction patterns are used by the FPGA to move the charge around the OTA's and thereby eliminate or minimize certain types of noise/image degradation.

B. Low Level

1. The CPU Board must provide adequate throughput for data coming in from the FPGA Board and going out over the high speed link.
2. The CPU Board must provide adequate main memory to allow for buffering the data on the board, thereby easing communications protocol requirements.
3. DMA transfers from the FPGA Board via FPGA Board controlled data transfers are necessary in order to minimize the usage of the CPU (CPU resources will likely be needed for the high-priority task of calculating the reference objects centroid and producing clocking patterns based on those calculations).
4. The CPU Board must provide an interface and protocol for interfacing with the PixelServer system and it's software.
    a. Ideally this interface would be via a TCP/IP socket connection. This would simplify the software development on the CPU Board considerably.
    b. Whatever interface to the PixelServer is implemented, it must not require excessive CPU resources on the CPU Board (CPU resources will likely be needed for the high-priority task

of calculating the reference objects centroid and producing clocking patterns based on those calculations).

5. The CPU Board must provide enough resources for calculating the centroid of the reference object, generating a clocking pattern from the results of those calculations, and moving the clocking pattern to the FPGA Board, all at the desired frequency (30hz? ie. 30 corrections per second?).

6. The CPU Board must provide a separate 10/100 ethernet connection for interacting with an Instrument Controller system.

7. The CPU Board should run Linux, and preferably have Linux already ported for it.

8. The CPU Board may need to be supported by RTAI or similar RTOS.

II. Software Requirements:

A. The software will provide an interface to the FPGA Board.

1. The software must provide driver code for setting up DMA transfers from the FPGA Board.

2. The software must provide driver code for interacting and setting up the FPGA Board, including sending over clocking patterns both for generating normal data and for generating data to be used for centroid correction.

3. Depending on the FPGA Board, the software may be required to control the FPGA Board, programming the FPGA, and essentially perform all FPGA Board functions (in the case that the FPGA board is not microprocessor based).

B. The software must provide support and protocol implementation for whatever data transfer interface is established between the IOTA and the PixelServer systems.

C. The software must process centroid correction operations.

1. The software must process image data.

a. The software must descramble the raw data (it is unlikely that data will come from FPGA board/OTA in a linear form).

b. The software must calculate the centroid of the descrambled data.

c. Based on the results of the centroid correction calculations, the software must generate a clocking pattern and send that pattern to the FPGA board.

2. The rate or frequency of processing sessions must meet requirements. This implies that the centroid correction task may require real-time support from the OS.

D. The software must provide a debugging interface for hardware, both on the FPGA Board and on the CPU Board itself.

E. The software must provide an interface to the Instrument Controller system.

1. Preferably this interface would be CORBA based.

2. This interface may instead be based on UNIX Sockets

FPGA Board

I. System Requirements

A. High Level

1. The board will drive and read data from a set of 4 OTA's

2. The board will pass the data read from the OTA's to another device via PCI.

B. Low Level

1. The board will provide support functionality for it's FPGA which will be the interface to the OTA's.

a. The board must be able to program the FPGA

b. The board must be able to access FPGA registers, be able to write to those registers, and be able to read those registers.

c. The board must be able to correctly set up the FPGA register space for different operations.

d. The board must be able to write clocking patterns to a memory space that is accessible to both the FPGA and the CPU.

2. The board will provide support functionality for mastering the PCI bus it is attached to, and writing data to the controller boards memory space.

3. The board must provide some interface for receiving clocking patterns. This may be via the PCI bus or via a different route.
4. The board must provide serial terminal ports and JTAG ports for debugging.

Software Requirements:

A. The software will provide an interface for the FPGA.
   1. The software must provide for programming and reprogramming the FPGA.
   2. The software must provide an interface for correctly setting up the FPGA control registers.

B. The software will provide an interface for writing clocking patterns to the memory space shared with the FPGA's.
   1. This will likely require setting up the FPGA to allow CPU access to the memory space.

C. The software will be required to set up DMA transfers over the PCI bus to the controller board.
   1. This will likely require setting up hardware to perform the actual task, but this is as of yet unclear.

D. The software must provide a peek-and-poke interface for debugging.

6.Conceptual Design

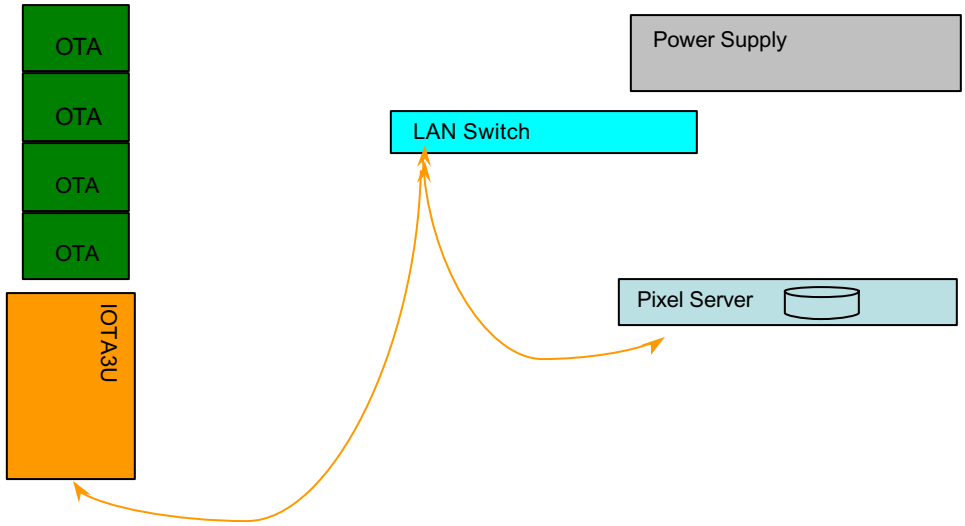
6.1.1. Design Philosophy

The stated design philosophy for the electronics design is:

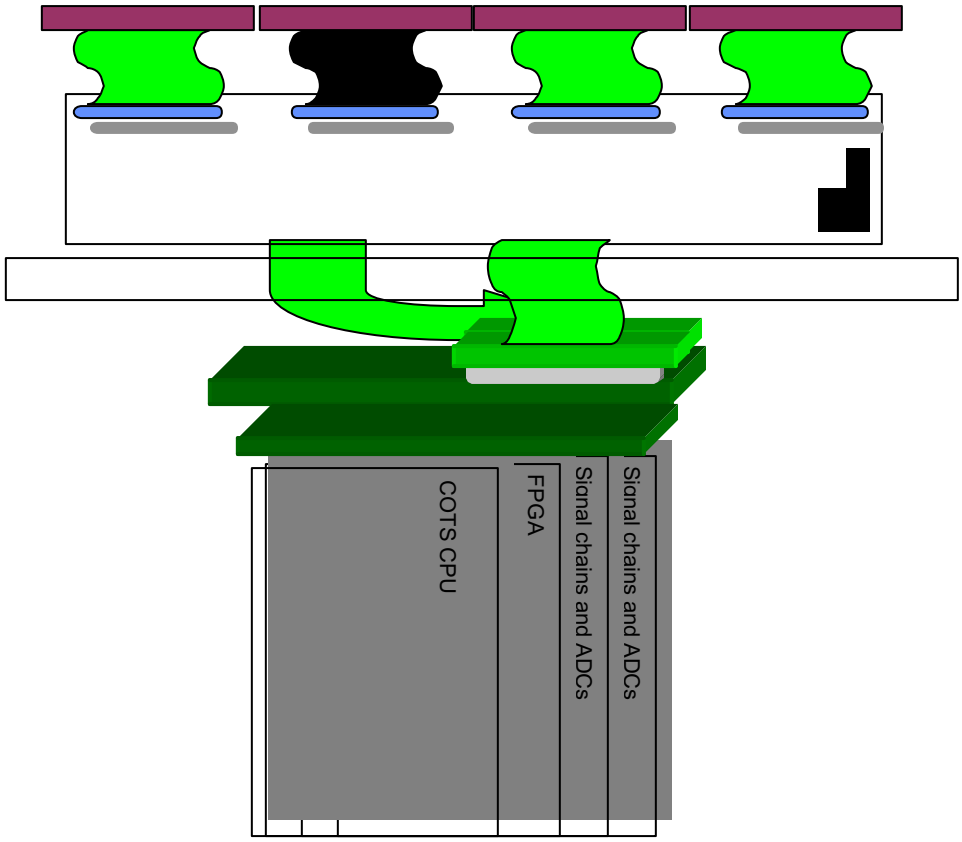
Use Commercial Off the Shelf (COTS) products whenever possible.
Look for second or alternate technology sources for products.
Look for technology areas where heavy competition creates technology advances.
Use economy of scale.
Choose most ubiquitous standards and interfaces to leverage additional available support.
Use “standards based” components whenever possible.

6.1.2. “Pre-CoDR” design

The basic building block of the scalar system would be a 1 x 4 array of OTA’s with an “IOTA” electronics controller and its corresponding Pixel Server. A whole 32K x32K focal plane would be composed of these buildeding blocks.

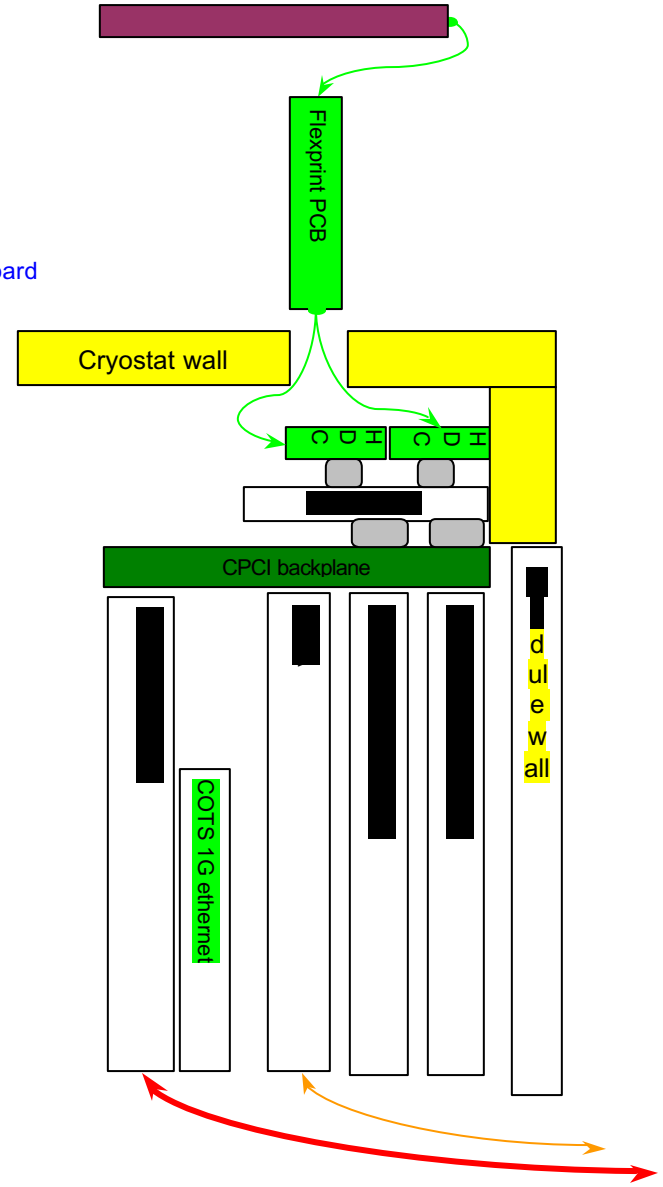


A 1x 4 array of OTA's will be supported by a set of electronics that are intended to closely fit in the physical space directly behind the array and connected via a flex-ribbon assembly that passed through the cryostat wall.

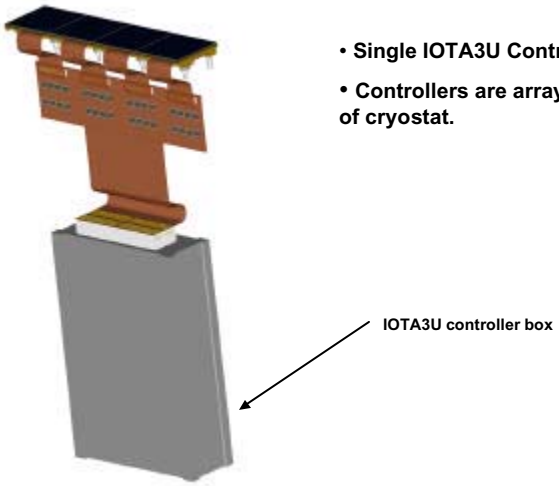


- Green areas are custom designed
- Blue areas are COTS
- 3U hardware could include connectors, front panels, guide rails, cooling components, chassis parts, etc

- COTS CPU board
  - Baseline LINUX based PowerPC
  - 1 or 2 channel 1G Ethernet fiber PMC daughterboard
  - CPCI bus interface
- FPGA3U board
  - CPCI interface
  - FPGA
  - Buffer memory
  - Data interface to DAQ3U
- DAQ3U board
  - Data interface
  - FPGA
  - Buffer memory
  - Signal Chain and ADCs
- Backplanes
  - CPCI Backplane, Interface Backplane

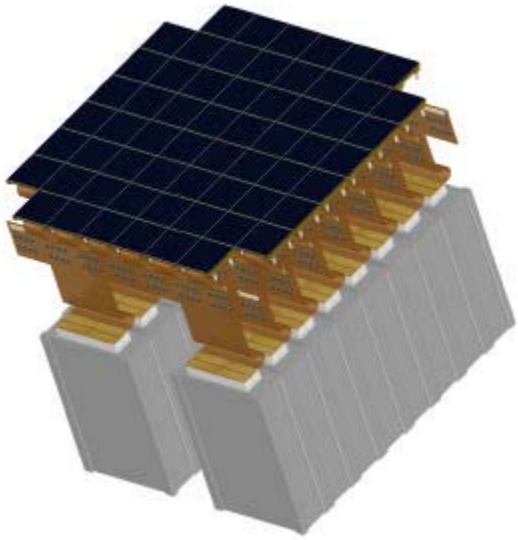


OTA Controller/Focalplane Relationship



- Single IOTA3U Controller operates 4 OTAs
- Controllers are arrayed behind back wall of cryostat.

Gigapixel Camera Controller Electronics

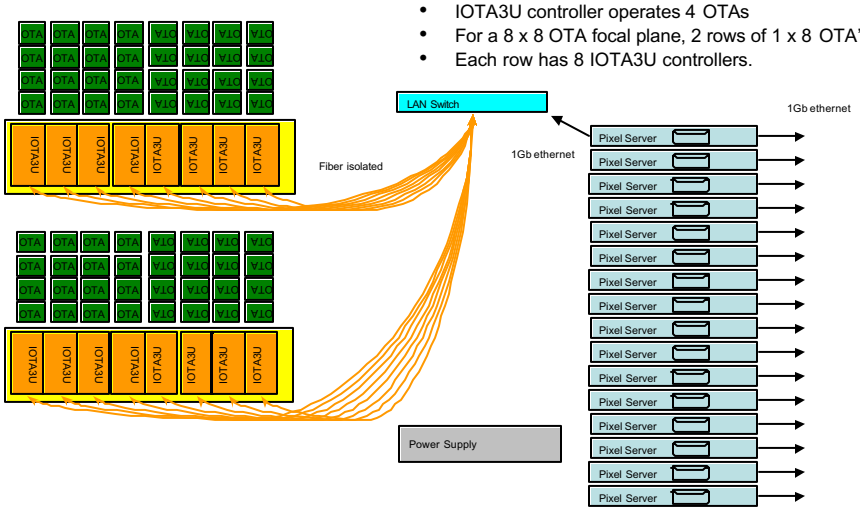


- Controllers are mounted behind cryostat.
- 16 controllers per Gigapixel camera.

Baseline Controller Design

2-row OTA Controller "Rack"

- IOTA3U controller operates 4 OTAs
- For a 8 x 8 OTA focal plane, 2 rows of 1 x 8 OTA's
- Each row has 8 IOTA3U controllers.



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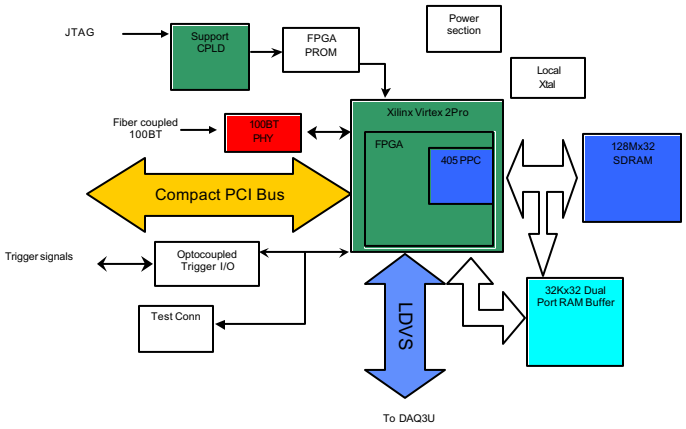
FPGA3U Board Design



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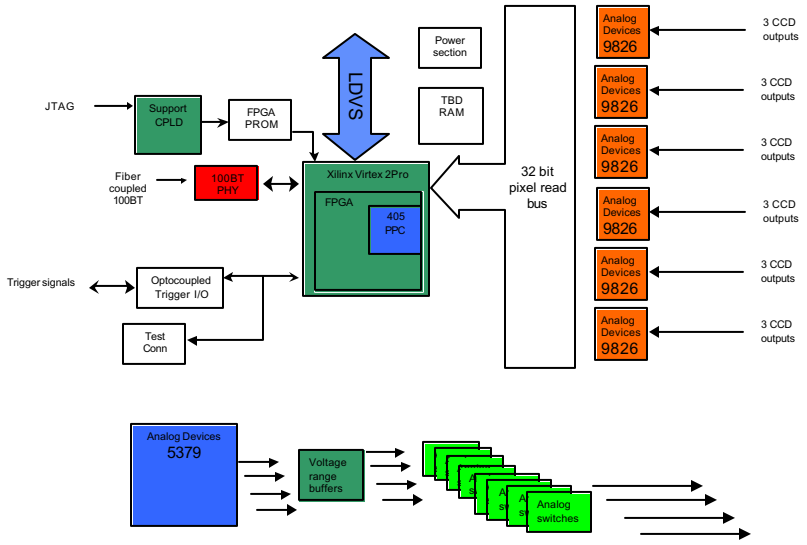
DAQ3U Board Design



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As presented, the system (single telescope) power maybe underestimated depending on the type of COTS CPU used. Intel Pentium family solutions can be factors of X4 more than PowerPC, ARM or MIPs based products. The following slide needs to be revised once a selection is made.

System Power Estimate

On-Telescope, Single Gigapixel Camera Electronics Controller

SYSTEM ESTIMATE:POWER DISSIPATION										
	PER BOARD (AMPS)				# parts	PER SYSTEM (AMPS)				
	[+3.3V]	[+5V]	[+12V]	[-12V]	count	[+3.3V]	[+5V]	[+12V]	[-12V]	
ADCs		0.08			96	0	0	0	0	
DACs		0.005	0.04	0.04	16	0	0	0.64	0.64	
FPGAs	0.50	0.50	0.00	0.00	48	24	24.00	0	0	
COTS CPU	0.66	1.6	0.05	0.05	16	10.56	10.56	0.8	0.8	
Misc	0.25	0.20	0.25	0.25	16	4	3.2	4	4	
					AMPS	38.56	37.76	5.44	5.44	
					WATTS	127.25	188.80	65.28	65.28	**446.61**

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7. Development Phase

The development phase of the plan is a distinct and separate phase of the project with a different set of critical drivers than the production phase.

The end goal of the Development phase is to design and produce a detector controller capable of running a 1 x 4 assembly of OTA's in a form factor suitable for testing in a laboratory and on a telescope

7.1. Estimated Staffing

Presently, there are less than 3FTEs working on the OTA controller development. We plan to use contract or consulting engineers rather than long term hires to provide narrowly focused and industry standard parts of the design to take advantage of high experience levels. The areas that need to be addressed during the development phase are:

- Software development = 2FTE, SW Engr (Charles Lockhart), 2nd TBD
  - Linux OS port to FPGA board – "industry standard" * possible contract SW engineer
  - Centroid calculation + pattern generation
  - 1 G ethernet benchmarking
  - Possible Real Time OS port/coding -"industry standard" * possible contract SW engineer
  - CORBA interface and coding - "industry standard" *possible contract SW engineer
- Hardware development = 2FTE, HW Engr (Peter Onaka), 2nd TBD
  - FPGA design
    - PCI interface – "industry standard" * possible contract HW engineer
    - Clocking state machine
    - ADC/DAC interfaces
    - Trigger design
  - PCB design
    - High speed digital layout – "industry standard" * possible contract HW engineer
    - Analog layout
- Electronics Assembly = 1 FTE Electronics Technician, Greg Ching.

The plan therefore calls for ~5FTEs, including consultants. This is a minimum staffing level for the development phase and should be augmented if qualified personnel can be found. **Note: a detailed task list and estimate will be added in an appendix.**

7.2. Milestones

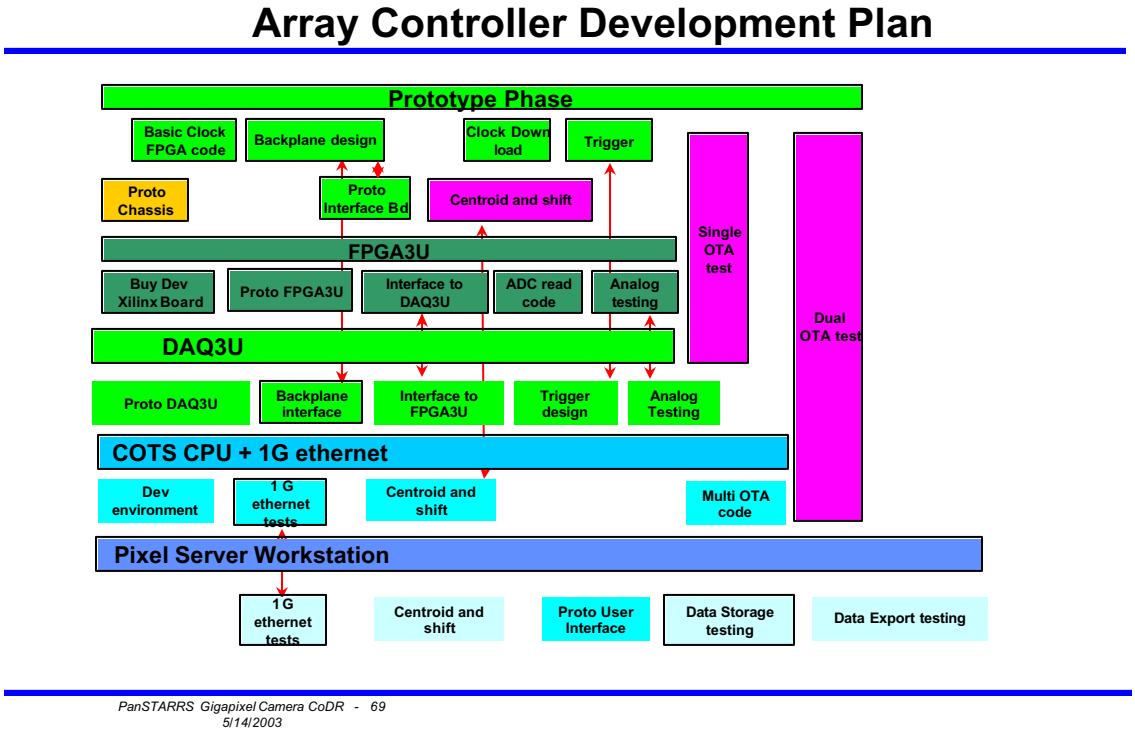
- Requirements derivation
- Conceptual design
- Development Plan
- Infrastructure setup
- Development system work
  - Specify and Assemble
  - Metrics testing
  - Hardware and software development
- Custom components
  - Design
  - Fabricate
  - Test and integrate
- Testing
  - Centroid OTA clocking benchtest
  - ADC analog testing
  - DAC testing
- System integration
  - Interface identification

- Technical interchange meetings
- Interface control documents

- Project requirements
  - Milestone identification
  - Scheduling
  - Cost estimates and tracking
  - Infrastructure and resource management
- Technical oversight
  - Review and approval

7.3. Schedule

NOTE: replace with detailed estimate:
Rough estimate:
Development System acquire/setup + lab setup = 1 month
Software and Hardware eval of FPGA ML300 system = +3 weeks
Design of FPGA and DAQ PCBs = +2months
Fabrication of FPGA and DAQ PCBs = + 5weeks
Baseline VHDL code finished for FPGA = + 1 month
DAQ board read for analog testing = +2 weeks



7.4. Development System

To arrive at a scalable and cost effective design, we plan to assemble a development system that will be a test bed for software and hardware solutions. Some of the hardware for this system may not be used on the actual final camera systems and do not have to comply with the final physical size requirements. We plan to later use this equipment in a permanent lab system to test the final production boards and develop follow-on software. The following is a list of proposed hardware and software for the Development system.

7.4.1. Tracewell Compact PCI powered test rack

The T-Frame ™ for CompactPCI is an 8-slot benchtop system platform for board level and software development, manufacturing and test. It will provide power for the CPU and FPGA portions of the system as well as the CompactPCI Backplane bus. Requirements are:

- open-frame design to eliminate extender boards
- Voltage, current and temperature monitoring
- Margin control for +5 and +3.3 volt outputs
- Hot-Swap compatible per PICMG 2.1
- 350 watt, N+1, or 700 watt operation
- Plugging power supplies with PFC and hot-swap
- IEEE 1101.10/11 compliant steel subracks to eliminate flex
- Adjustable rear cardcage for 60, 80, and 100mm boards

Vendor: **Tracewell Systems, Inc-** *Ohio Location*
567 Enterprise Drive
Westerville, Ohio 43081

Part type: 580-6001-F00-00
Approximate Cost: $ 3,595.00
Info: www.tracewell.com

7.4.2. Xilinx FPGA development hardware and software

We will be using a new generation of Field Programmable Gate Array (FPGA) on this project to meet the small space available for the electronics. The Xilinx VirtexII family of parts has been identified as a good candidate for this design. These integrated circuits are firmware programmed using software development tools provided by Xilinx. The requirements for the development software are:

Device support for VirtexII family
VHDL synthesizer
Floorplanner
Timing Driven Place & Route
IBIS Models

When using the VirtexIIpro parts there are additional requirements:

GNU Embedded Tools

GCC-GNU Compiler
GDB-GNU Software Debugger

We should be able to qualify for the educational pricing through the Xilinx University Program (XUP) for the necessary software packages which are:

ISE Foundation cost $595 (regular cost $2,495), each additional license is $290.
Embedded Development Kit XUP cost:$200 (regular cost $495)

*There is a yearly extension charge for the software of $250 for the first license.

We plan to purchase 3 licenses.

A vendor hardware development platform is used for both software and firmware development with the FPGA. This is another purely developmental piece of hardware and will not be used in the final camera systems. The requirements for a hardware development platform are:

Connector
32 / 33 PCI Mezzanine Card slot with PMC Conn4

Interface
10 / 100 Ethernet
4 ports of Optical Gigabit Ethernet (serial transceiver)
2 - RS232
JTAG port
Serial port
IEEE1284 Parallel port
SPI EEPROM

Memory
128 MB DRAM DDR

Operating System

Xilinx Family
Virtex-II Pro

The ML300 Evaluation Platform meets the requirements. One system would be ordered.

Part number:DO-V2P-ML300
cost: $4,695.00

7.4.3. Pixel Server Linux PC with 1 Ge

We will need a reasonable emulator for our Pixel Server platform. We do not necessarily need the small form factor ofof the final platforms, but the processing power and throughput should be comparable.
Requirements: Minimum Dual >1.24Ghz class P4 or Xeon with 1Ge interface – Linux compatible
Manufacturer: Various
Part: Various
Cost~$4,000

7.4.4. Software development Laptop

Powerful laptop with large display as our build environment. Our debugging and development tools require a large amount of room on
the screen, and at least 1280x1024 screen resolution. Unfortunately the standard 14"-15" inch laptop screens generally don't have that good a resolution and when they do everything is too small for viewing. We need the build environment to be easily portable between the lab and our offices. Also, cross compiling requires a more powerful processor and more memory than compiling on a host machine, and we'll be supporting build environments for multiple processors.

We're looking at the Sony GXX series laptops, and have found a suitable one, the GRV680, available.

Manufacturer: Sony
Part: GRV680
Cost: $2,600

7.4.5. 1 Gigabit Switch

We will need to benchmark the performance of the embedded 1Ge network interface to the user /developer PC.
Requirements: Fiber and possible copper 1Ge ports.
Manufacturer: TBD
Part: TBD
Cost: TBD

7.4.6. Software JTAG Interface BDI2000.

This is a JTAG interface from Abatron that facilitates debugging and development on several different embedded processors (http://www.abatron.ch/BDI/bdihw.html#anchor1192267). This is a particularly needful thing since we're probably not going to be purchasing the MV license, and we may need to use RTAI. I'm currently looking into price and availability.
Manufacturer: Abatron
Part :
Cost:

7.4.7. COTS CPU board

There are several vendors being looked at presently. We may need to purchase products from more than one vendor to fully evaluate the performance and software development environment. The primary function of this part is to collect the science image data, do the TCP/IP formatting and export the data out of a 1 Gigabit ethernet port (all at high speed).
Manufacturer#1 :
Part:
Cost
Manufacturer#2:
Part:
Cost:

7.5. Critical Analog/Digital Component Evaluation

Achieving actual noise vs. speed performance from two key analog/digital components is critical to meet the system sensitivity and speed specifications. These two components are:

The Analog to Digital converter (ADC). Two sample baseline parts, Analog Device's ADC9826's have been received. A small test PCB will be designed and placed in a previous generation system to benchmark the delivered performance.

The Digital to Analog Converter (DAC). Another Analog Devices part AD5379 is not sampling yet but has the desired small size and high channel count needed for the clock and bias voltages. Contact with the manufacturer has been made to determine the release date and availability of parts and an evaluation kit.
Estimated cost for evaluation board: $600

Three small PCBs will be designed to hold these critical parts and tested in existing systems.
Estimated cost for PCBs: ~$1,800 each.

7.6. Fabrication Plan

We intend to make use of outside commercial manufacturer (CM) companies for the assembly of the high density electronics PCB's. This approach is not without it's own problems, however. CMs generally require a minimum purchase amount or number of assemblies, documentation must be complete and unambiguous, and component ordering and kitting adds complexity to the process.
The plan is to develop a working relationship with a few CMs during the Development Phase to smooth out problems for the Production Phase. Concurrent with this outside work, we intend to augment our internal IfA capability to be able to test and rework PCBs in house. This in house capability is essential because despite the fact that the CMs will be tasked with assembling the PCBs, we will not have all the firmware developed for the programmable parts (FPGAs) unitl after receipt of the PCBs (i.e. the CMs cannot fully test the boards).

7.7. Laboratory Infrastructure

7.7.1. BGA Assembly and Inspection

The IfA (and specifically, the IRTF) has already invested money in electronics production equipment. The IfA currently has the capability to assemble, inspect, test and rework surface mount components in the TQFP (Thin Quad Flat Pack) and OFP (Quad Flat Pack) packages. The IOTA PCBs will require the use of BGA (Ball Grid Array) packages because this packaging approach provides higher circuit density, and some devices are not available in another style. The following figure shows the two package types and illustrates the inspection problem imposed by the BGA approach. The BGA soldered contacts are located completely under the component package in a grid layout which makes visual inspection impossible with standard microscopes.

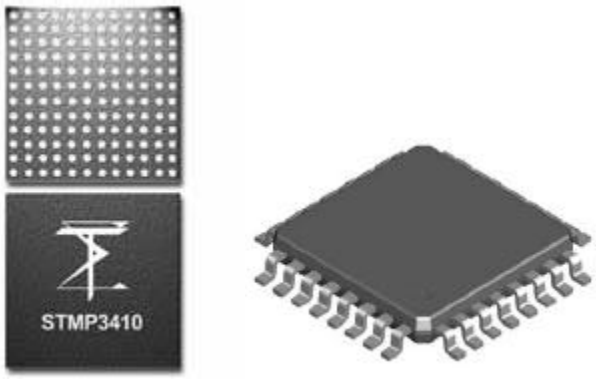


Figure: BGA (bottom and top view) vs. TQFP

There are 2 complimentary ways to do proper inspection of the BGA solder connections, X-ray imaging and specialized inspection microscopes. We intended to purchase both systems to provide high quality inspection. The next figures show the outputs from an X-ray inspection system and specialized microscope.

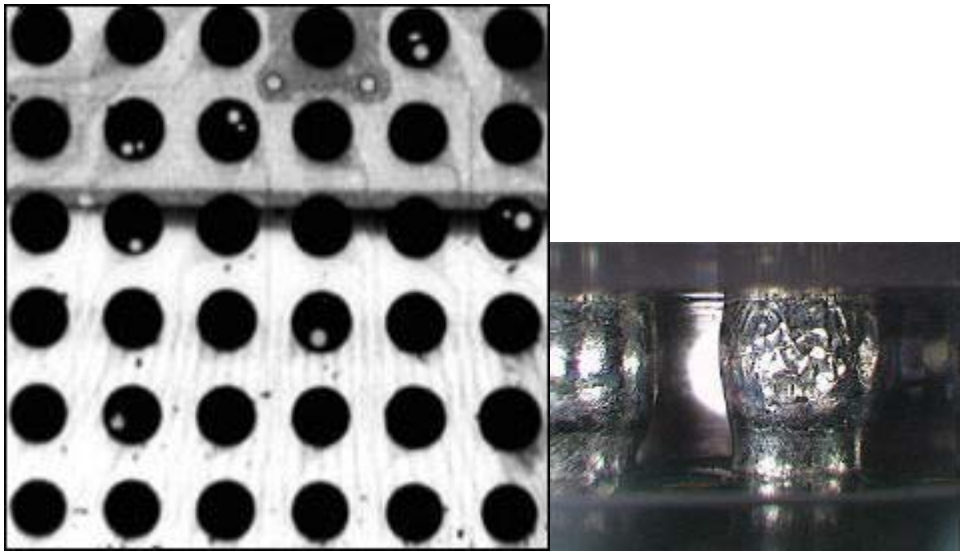


Figure: X-ray and microscope views

7.7.1.1.1. X-ray BGA inspection System

Manufacturer: TBD
Part number: TBD
Cost: TBD

7.7.1.1.2. BGA inspection microscope

Manufacturer: ERSA
Part number: TBD
Cost: ~$16,000

7.7.1.1.3. Vacuum oven

Modern BGA ICs are susceptible to moisture absorption. An explanation follows:
“One particularly costly example of moisture-related damage is the "popcorn" effect that occurs during reflow soldering of IC packages.
Although the vast majority of integrated circuits are packaged in plastic encapsulants (because they are cheaper than ceramic ones), manufacturers are often unaware of the consequences of using hygroscopic materials in a solder reflow process. Moisture absorbed into the package vaporizes during the rapid heating and generates pressure along the metal-to-plastic contact regions. Differences between the coefficients of thermal expansion of the two materials can cause loss of adhesion, swelling, and cracking. An audible "pop" signals the problem, and testing confirms a deterioration of electrical function.”

The only way to “revive” the component after it has absorbed moisture is to desiccate in it a vacuum oven.
Manufacturer:
Part:
Cost:

7.7.1.1.4. Desiccating Storage

Before the components are vapor flow soldered to the PCBs, it is important to store them in an appropriate low humidity container. Nitrogen controlled setpoint desktop cabinets are requested.
Manufacturer: Terra Universal
Part: Plastic SmartDesiccator 1911-23
Cost: $1,900

7.7.1.1.5. Static Safe Laminar Flow Hood

The soldering and assembly area for the PCB's should be located in a static safe laminar flow area to assure quality control.
Manufacturer: TBD
Part: TBD
Cost: TBD

7.7.2. Test Tools

The following list of general test tools will be necessary to provide a dedicated test station for the PCBs being developed.

7.7.2.1. System Power Supply

Requirements: 5 or more output capability for the system voltages (+3.3V,+5V,+/-12V,+24V),
Voltage and current displays, overvoltage and overcurrent shutdown, simultaneous power on, rackmount.
Manufacturer: Agilent Inc.
Part: 66000 system rack with power modules and programming keyboard
Cost: ~$3,500

7.7.2.2. Bench Test Power Supply

Requirements: At least 3 or more output capability for the system voltages (+3.3V,+5V,+/-12V,+24V),
Voltage and current displays, overvoltage and overcurrent limit, simultaneous power on.
Manufacturer: Agilent
Part: E3631A
Cost: $1,200

7.7.2.3. Digital Oscilloscope

The two closest candidates that the IfA has both have broken displays. The DSO will be used to diagnose analog and digital problems with the OTA signals and the digital processing chain.
Requirements: 4 channel digital storage, 500Mhz bandwidth, >2.5Gsps, FFT analysis
Manufacturer: Tektronix
Part: TDS3054B
Cost: $10,000

7.7.2.4. PC Hosted Logic Analyzer

We have found the lower cost PC hosted logic analyzers to be excellent for documentation of digital signals and this capability makes up for some of their lower performance (lower channel count and speed).
Requirements: minimum 34 channels, min 100Mhz, small form factor.
Manufacturer: Agilent
Part: E9340A
Cost: $3,200

7.7.2.5. Bench Data Acquisition Unit

A general purpose way of measuring multiple signals and generating test stimulus is needed to test the PCBs.

Requirements: DC and AC measurement capability, switched multichannel input, analog signal generation.
Manufacturer: Agilent
Part: 34970A with 34908A,34907A and 34903A modules and USB to GPIB adapter
Cost: $2,900

7.7.2.6.Inspection Microscope

A general purpose stereo microscope is needed for PCB, connector, and flexprint inspection.
Requirements: Stereoscopic, wide field, long working distance, boom mount.
Manufacturer:
Part:
Cost:

7.7.2.7.Function/Arbitrary Waveform Generator

Requirements: Sine, square, triangle, ramp, noise, sin(x)/x waveforms. Greater than 10Mhz, linear and log sweep.
Manufacturer: Agilent
Part: 33120A
Cost: $1,800

7.7.2.8.Cryogenic Temperature Controller

We will be operating and controlling the temperature of the OTAs in a cryogenic environment. A servo temperature controller (based on a cryogenic temperature sensor) is needed.
Manufacturer: Lakeshore Cryotonics
Part: Model 332 controller and calibrated Si diodes
Cost: $2,000

7.8. Quality Control/Assurance

The electronics QC will be implemented in the 3 level test standard of the IRTF for each major subassembly.
Each PCB is identified with a serial number plus test label, and undergoes predefined written tests (customized for each PCB type).

- Bench test – Single PCB test with simple bench test tools (power supply, function generator, DSO etc) that verifies non-software related functionality.
- Level 1 – depending on the PCB type, this test will involve the use of test software of actual operational software in the Development system. Typically data flow and functional specifications can be tested. To make this test more comprehensive, and engineering grade OTA assembly should be used.
- Level 2 – denotes a full performance and functional test of the Assembly in an actual camera system (OTAs at operational temperature).

PCB assemblies will b not be used in an actual camera system until they have passed at Level 1 and any failures will cause the board to be retested from scratch.

7.9. Purchase Generation and Tracking Database

We will be using a copy of the IRTF's Filemaker pro database for purchasing. This is a "shadow system" to the RCUH FMIS purchasing database which does not provide adequate access, search and detailed information for our use. The purchase database actually consists of several interrelated databases and is served by a single machine (host). The databases and their functions are:

1. Purchase database:
    a. Requisition Form (Univ. of Hawaii)

   b. Requisition Status
   c. Annual Report
   d. Record of Verbal Quotations
   e. RCUH Record of Verbal Quotations
   f. Request for Sole Source Form
   g. RCUH Sole Source Form
   h. Inventory Control Form (newer)
   i. Inventory Control Form (old)
   j. UH form 39, Authorization to Purchase Equipment with Federal Contract or Grant Funds
   k. PPMO Form 95, Cost or Price Reasonableness
   l. Purchase Order Change Form
   m. Request for Price and Availability
   n. Request for Quotation (short)
   o. Request for Quotation (long)
   p. Request for Quotation Terms and Conditions
   q. RCUH Sole Source Form
2. Accounts database
   a. Listing of account ID, account code number, project title, authorized signature, title, contract grant #, termination date and admin officer.
3. Authorization for Payment
   a. UH authorization for payment form
   b. RCUH authorization for payment form
4. Purchase Authorization database
   a. UH PA form
   b. Additional itemization list
   c. Certificate for Reimbursement
5. Staff database
   a. Phone list + contact info
6. Vendor database
   a. Quick lookup
   b. Contact Info
   c. Vendor Qualification
   d. Data entry
7. Individual Bill Of Materials for each electronics subassembly
   a. BOM
   b. BOM cost
8. Master Parts List

The database can accessed from Manoa and Hilo using the Filemaker pro software on both Windows and Mac platforms. Once the program is loaded, using the "open an existing file" command and specifying the host name will allows one to open the purchase database. There are pull-down menus for the vendor and account fields and auto-fill-in fields based on the other databases in the directory.

7.10. Document Tree

We will use our IRTF standard numbering system for components and subassemblies:
900 level document will detail the system level.
800 level documents will identify and detail major subsystems (e.g. Temperature control, IOTA controller).
700 level documents will identify and detail subassemblies, typically finished PCB's.
600 level documents will identify and detail cable subassemblies.
500 and lower numbers are used for components.

Actual numbers will be assigned and checked into the Master Parts List database.

7.10.1.Development Directory

Typically a regularly backed up server will host the project directory tree where each major subassembly will have a subdirectory under the main project directory. Each subassembly will have a standard set of subdirectories:

1. Drawings
2. Text
3. Photo
4. Database

Every team member should used

8.Production Phase

We will hold an internal review at the end of the Development Phase to determine the level of success achieved and identify necessary changes. A Production Phase will follow that will not simply recreate the previous system. Instead, the design will be modified to incorporate recent technological advances, incorporate cost and maintenance engineering changes, and include the expansion of the system for data storage and deliver to the partner groups.